Amendments to the Claims

1. (Currently Amended) A silicon-on-insulator radiation detector, comprising:

a silicon layer formed on an insulating substrate, wherein the silicon layer includes a PNPN structure; and

a gate ~~layer~~ formed over the PNPN structure, wherein ~~the gate layer includes a PN gate~~ a PN interface of the gate is offset from a P-well - N-well interface of the PNPN structure; ~~and~~

wherein latch-up occurs in the radiation detector only in response to incident radiation.

2. (Currently Amended) The silicon-on-insulator radiation detector of claim 1, wherein the PNPN structure comprises a P+ region, an N-well, a P-well, and an N+ region, and wherein the ~~PN~~ gate comprises a first P+ region and a first N+ region.

3. (Original) The silicon-on-insulator radiation detector of claim 2, wherein the first P+ region of the gate covers the N-well of the PNPN structure and extends a substantial distance over the P-well of the PNPN structure.

4. (Original) The silicon-on-insulator radiation detector of claim 3, further comprising:

a parasitic PMOS FET within the radiation detector that is prevented from turning on by coupling the P+ region of the PNPN structure and the first P+ region of the gate to a source voltage; and

a parasitic NMOS FET within the radiation detector having a threshold voltage of about 1.2 volts, wherein the threshold voltage prevents the parasitic NMOS FET from turning on.

5. (Original) The silicon-on-insulator radiation detector of claim 2, wherein the first N+ region of the gate covers the P-well of the PNPN structure and extends a substantial distance over the N-well of the PNPN structure.

6. (Original) The silicon-on-insulator radiation detector of claim 5, further comprising:

a parasitic NMOS FET within the radiation detector that is prevented from turning on by coupling the N+ region of the PNPN structure and the first N+ region of the gate to ground; and

a parasitic PMOS FET within the radiation detector having a threshold voltage of about -1.2 volts, wherein the threshold voltage prevents the parasitic PMOS FET from turning on.

7. (Currently Amended) The silicon-on-insulator radiation detector ~~gate~~ of claim 1, wherein the gate ~~layer~~ comprises a PNPN gate, and wherein the PNPN gate includes a first P+ region, a first N+ region, a second P+ region, and a second N+ region.

8. (Original) The silicon-on-insulator radiation detector of claim 7, wherein the first N+ region of the PNPN gate is located over the N-well of the PNPN structure and the second P+ region of the PNPN gate is located over the P-well of the PNPN structure.

9. (Original) The silicon-on-insulator radiation detector of claim 8, wherein an interface between the first N+ region and the second P+ region of the PNPN gate is substantially coincident with an interface between the P-well and N-well of the PNPN structure.

10. (Original) The silicon-on-insulator radiation detector of claim 8, further comprising:

a parasitic PMOS FET within the radiation detector having a threshold voltage of about -1.2 volts, wherein the threshold voltage prevents the parasitic PMOS FET from turning on; and

a parasitic NMOS FET within the radiation detector having a threshold voltage of about 1.2 volts, wherein the threshold voltage prevents the parasitic NMOS FET from turning on.

11. (Currently Amended) A radiation detector, comprising:

a silicon-on-insulator PNPN diode structure and a gate formed over the PNPN diode structure, wherein a PN interface of the gate is offset from a P-well - N-well interface of the PNPN diode structure, wherein latch-up occurs in the radiation detector only in response to incident radiation.

12. (Currently Amended) The radiation detector of claim 11, ~~further comprising:~~

~~a PN gate over the PNPN diode structure,~~ wherein at least one parasitic FET within the radiation detector has a threshold voltage of about 1.2 volts or -1.2 volts.

13. (Original) The radiation detector of claim 11, further comprising:

a PNPN gate over the PNPN diode structure, wherein at least one parasitic FET within the radiation detector has a threshold voltage of about 1.2 volts or -1.2 volts.

14. (Currently Amended) An integrated circuit, comprising:

a silicon-on-insulator radiation detector, wherein the radiation detector includes:

a silicon layer formed on an insulating substrate, wherein the silicon layer includes a PNPN structure;

a gate ~~layer~~ formed over the PNPN structure~~, wherein the gate layer includes a PN gate~~ wherein a PN interface of the gate is offset from a P-well - N-well interface of the PNPN structure; and

wherein latch-up occurs in the radiation detector only in response to incident radiation.

15. (Currently Amended) The integrated circuit of claim 14, wherein the PNPN structure comprises a P+ region, an N-well, a P-well, and an N+ region, wherein the ~~PN~~ gate comprises a first P+ region and a first N+ region, and wherein the first P+ region of the gate covers the N-well of the PNPN structure

and extends a substantial distance over the P-well of the PNPN structure.

16. (Currently Amended) The integrated circuit of claim 14, wherein the PNPN structure comprises a P+ region, an N-well, a P-well, and an N+ region, wherein the ~~PN~~ gate comprises a first P+ region and a first N+ region, and wherein the first N+ region of the gate covers the P-well of the PNPN structure and extends a substantial distance over the N-well of the PNPN structure.

17. (New) A method for forming a silicon-on-insulator radiation detector, comprising:

forming a silicon layer on an insulating substrate, wherein the silicon layer includes a PNPN structure; and

forming a gate on the silicon layer and offsetting a PN interface of the gate from a P-well - N-well interface of the PNPN structure;

wherein latch-up occurs in the radiation detector only in response to incident radiation.